REMARKS

Claims 1-31 are pending in the case, of which claims 8-31 are withdrawn from consideration. Claims 1-7 are rejected. In the present submission, claims 1 and 5 have been amended. Reconsideration is respectfully requested.

§112 Rejection

Claims 1-7 are rejected under §112, second paragraph, as being indefinite. In the present submission, claim 1 has been amended to correct the typographical errors relating to "image processing pipeline." Furthermore, claim 5 has been amended to correct the claim dependency. Claim 5 now provides antecedent basis for the limitation "said image processing circuit." Claim 1 and dependent claims 2-7 now meet the requirements under §112 and withdrawal of the §112 rejection of claims 1-7 is respectfully requested.

§103a Rejection – Claims 1 and 7

Claims 1 and 7 are rejected under §103(a) as being unpatentable over Horii et al. (USP 6,573,931; hereinafter "Horii") in view of Yamada et al. (USP 5,995,137; hereinafter "Yamada") and further in view of Fowler (USP 5,461,425). The Examiner contends that Figure 7 and related descriptions of Horii describes substantially all limitations of claims 1 and 7 except for selecting from a group of video formats and a sensor array of digital pixels. The Examiner relies on Yamada and Fowler for reciting selecting different video formats and digital pixels. Applicant respectfully traverses the rejection.

Horii describes in figs. 1 and 7 a video input apparatus where a video input unit 100 is connected to a video processing unit 200 through a cable 109. The video input unit of Horii does not include any memory buffer for storing the pixel data. Instead, Horii states specifically that the "data multiplexing and demultiplexing unit 115 multiplexes the video signal 114 and control data from the system control unit, and transmits multiplexed data to the image processing unit 200" (Horii, col. 2, ln. 1-5). Therefore, the data multiplexing and demultiplexing unit 115 does not act as an image buffer for storing pixel data as the Examiner contends. Horii describes multiplexing the image data and the control data and transmitting the multiplexed data on the same bus 109.

Claim 1

Claim 1, as originally filed, recite a digital image sensor including an image buffer for storing the pixel data and a pixel bus for transferring pixel data and a control interface bus for transferring control information. As shown in Figure 1 and described in paragraphs [0041]-[0042] of Applicant's specification, the pixel bus and the control interface bus are separate busses. To the contrary, Horii does not include any image buffer in the video input unit and more importantly, Horii describes using the same bus to transmit pixel data and control information by use of multiplexing.

Nonetheless, Applicant amends claim 1 to further clarify the claim. As amended, claim 1 now recites that the "control interface bus [is] coupled between said first interface circuit and said second interface circuit and [is] separate from said pixel bus." Horii **does not** teach or suggest at least this limitation of claim 1. In fact, Horii **teaches away** from using separate bus but instead teaches using the same bus to transfer the image data and control data by multiplexing the image data and control data. Yamada and Fowler **do not** cure the deficiency of Horii. Claim 1 is therefore patentable over all of the cited references.

Claim 7

Claim 7, dependent upon claim 1, is patentable over the cited references at least for the same reasons claim 1 is patentable.

For the above reasons, withdrawal of the §103(a) rejection of claims 1 and 7 is respectfully requested.

§103a Rejection – Claims 2-6

Claims 2-6 are rejected under §103(a) as being unpatentable over Horii in view of Yamada and further in view of Fowler and further in view of Tamama.

Claims 2-6, dependent upon claim 1, are patentable over the Horii, Yamada and Fowler at least for the same reasons claim 1 is patentable. Tamama does not cure the deficiency of Horii, Yamada and Fowler. Claims 2-6 are therefore patentable over all of the cited references. Withdrawal of the §103(a) rejection of claims 2-6 is respectfully requested.

Rejoinder of Withdrawn Claims

Applicant submits that in the office action of February 28, 2007, Examiner indicated that claim 1 links inventions I to VI of claims 2-31 and Examiner states that claims 8-31 are eligible for rejoinder when claim 1 is indicated to be allowable. Claims 8-31 depend from claim 1 and therefore include all the limitations of claim 1. For the reasons stated above, claim 1 is in condition for allowance. Therefore, rejoinder of claims 8-31 is respectfully requested. Claims 8-31, dependent upon claim 1, are patentable over the cited references at least for the same reasons claim 1 is patentable.

CONCLUSION

Claims 1-31 are pending in the present application, of which claims 8-31 are withdrawn from consideration. In the present submission, claims 1 and 5 have been amended. Claims 1-7 are in condition for allowance. Since claim 1 links the inventions of claims 2-31, withdrawn claims 8-31 are eligible for rejoinder and rejoinder of claims 8-31 is respectfully requested. If the Examiner would like to discuss any aspect of this application, the Examiner is invited to contact the undersigned at (408) 382-0480.

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I hereby certify that this correspondence is being submitted electronically to the United States Patent and Trademark Office using EFS-Web on the date shown below.

/Carmen C Cook/	January 6, 2008
Attorney for Applicant(s)	Date of Signature

Respectfully submitted,

/Carmen C Cook/

Carmen C. Cook
Attorney for Applicant(s)
Reg. No. 42,433
Patent Law Group LLP
2635 N. First St.
Suite 223
San Jose, CA 95134
Tel (408) 382-0480 x208
Fax (408) 382-0481